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Depletion-mode Ga_2O_3 metal-oxide-semiconductor field-effect transistors on β-Ga_2O_3 (010) substrates and temperature dependence of their device characteristics

Masataka Higashiwaki,[1,a)] Kohei Sasaki,[1,2] Takafumi Kamimura,[1] Man Hoi Wong,[1] Daivasigamani Krishnamurthy,[1] Akito Kuramata,[2] Takekazu Masui,[3] and Shigenobu Yamakoshi[2]

[1]*National Institute of Information and Communications Technology, 4–2–1 Nukui-Kitamachi, Koganei, Tokyo 184–8795, Japan*
[2]*Tamura Corporation, 2–3–1 Hirosedai, Sayama, Saitama 350–1328, Japan*
[3]*Koha Co., Ltd., 2–6–8 Kouyama, Nerima, Tokyo 176–0022, Japan*

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Single-crystal gallium oxide (Ga_2O_3) metal-oxide-semiconductor field-effect transistors were fabricated on a semi-insulating β-Ga_2O_3 (010) substrate. A Sn-doped n-Ga_2O_3 channel layer was grown by molecular-beam epitaxy. Si-ion implantation doping was performed to source and drain electrode regions for obtaining low-resistance ohmic contacts. An Al_2O_3 gate dielectric film formed by atomic layer deposition passivated the device surface and significantly reduced gate leakage. The device with a gate length of 2 μm showed effective gate modulation of the drain current with an extremely low off-state drain leakage of less than a few pA/mm, leading to a high drain current on/off ratio of over ten orders of magnitude. A three-terminal off-state breakdown voltage of 370 V was achieved. Stable transistor operation was sustained at temperatures up to 250 °C. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4821858]

We have been proposing gallium oxide (Ga_2O_3) as a promising candidate for power device applications because of its excellent material properties and suitability for mass production.[1,2] With a wide bandgap of 4.7–4.9 eV,[3–5] the estimated breakdown electric field of 8 MV/cm for Ga_2O_3 is about three times larger than those of SiC and GaN. Ga_2O_3 can be controllably doped to obtain electron densities (n) from semi-insulating to as high as 10^{19} cm^{-3}.[6–9] The extrapolated experimental bulk electron mobility of Ga_2O_3 reaches a relatively high value of about 300 cm^2/V·s for $n = 10^{15}$–10^{16} cm^{-3}, which is typical for the drift layers of vertical power transistors and diodes.[10] This is supported by theoretical calculations showing that the electron effective mass of 0.23–0.34m_0 (m_0: free electron mass) for Ga_2O_3 is comparable to those for conventional widegap (3–4 eV) semiconductors.[5,8,11] The Baliga's power device figure of merit of Ga_2O_3 is estimated to be several times larger than those of SiC and GaN based on their material properties,[1] projecting higher breakdown voltages (V_{br}) and efficiencies for Ga_2O_3 power devices than their SiC and GaN counterparts. The other important attribute of Ga_2O_3 is that single-crystal bulk materials can be synthesized by using conventional melt growth techniques such as the floating-zone (FZ), the edge-defined film-fed growth, and Czochralski methods.[12–15] These technologies, which are currently employed for manufacturing sapphire substrates, will offer Ga_2O_3 a big advantage over other widegap semiconductors by enabling simple and low-cost mass production of single-crystal native Ga_2O_3 substrates. Therefore, Ga_2O_3 power devices have the obvious potential to surpass SiC and GaN in not only device performance but also cost effectiveness.

We have previously demonstrated Ga_2O_3 metal-semiconductor field-effect transistors (MESFETs) on single-crystal β-Ga_2O_3 substrates.[1] The MESFET showed excellent device characteristics such as a three-terminal off-state V_{br} of 250 V and a drain current (I_d) on/off ratio of about four orders of magnitude. However, the device suffered from high contact resistance of source and drain electrodes. In addition, its I_d on/off ratio was limited by a small leakage current through the unpassivated Ga_2O_3 surface. To address these shortcomings, we fabricated Ga_2O_3 metal-oxide-semiconductor FETs (MOSFETs) in the present work by adopting Si-ion (Si^+) implantation doping for improved ohmic contacts and atomic layer deposition (ALD) of a dielectric film for surface passivation and gate insulation. Temperature dependences of current–voltage (I-V) characteristics of the Ga_2O_3 MOSFETs were closely examined to estimate their capability for high-temperature application.

The depletion-mode Ga_2O_3 MOSFETs were fabricated on Fe-doped semi-insulating single-crystal β-Ga_2O_3 (010) FZ substrates. A 300-nm-thick n-Ga_2O_3 channel layer with a nominal Sn doping concentration of 7×10^{17} cm^{-3} was grown by molecular-beam epitaxy at a substrate temperature of 560 °C and a growth rate of 0.6 μm/h. Ga and Sn fluxes were, respectively, supplied by Ga metal and SnO_2 powder from conventional Knudsen cells. A gas mixture of ozone and oxygen was used as the oxygen source. The activation energy of Sn in Ga_2O_3 was estimated to be about 60 meV from the temperature dependence of n; therefore, a little less than half of the Sn dopants were activated in the Ga_2O_3 epitaxial layer at room temperature (RT). In fact, an effective carrier density (N_d-N_a) of about 3×10^{17} cm^{-3} was

a)Electronic mail: mhigashi@nict.go.jp

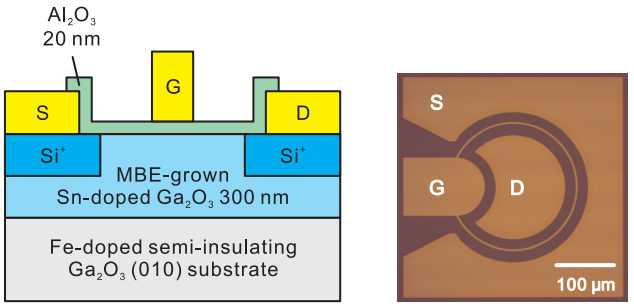


FIG. 1. (a) Schematic cross-section and (b) optical micrograph of depletion-mode Ga_2O_3 MOSFET.

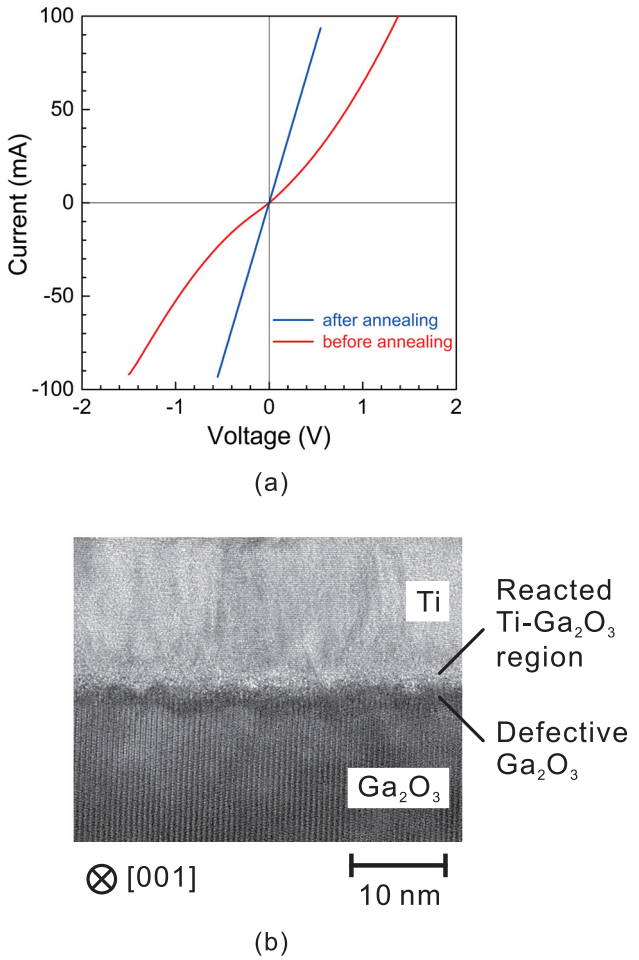
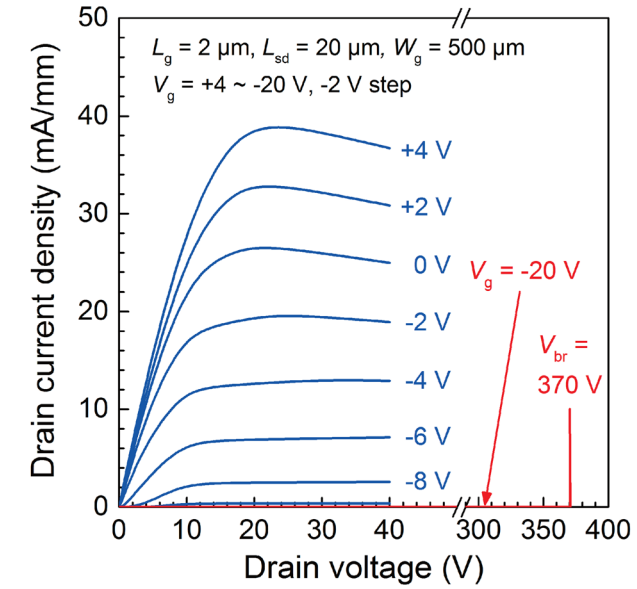


FIG. 2. (a) I-V characteristics of implanted Ga_2O_3 film before and after Ti/Au electrode annealing. The electrode separation was 24 μm. (b) Cross-sectional TEM micrograph of the Ti/Ga_2O_3 interface after annealing at 470 °C.

experimentally confirmed for the channel layer at RT by capacitance–voltage measurements on MOS diodes simultaneously fabricated on the same substrate.

Figures 1(a) and 1(b) show a cross-sectional schematic and an optical micrograph of the Ga_2O_3 MOSFET, respectively. We employed a circular FET pattern as shown in Fig. 1(b). Multiple Si^+ implantations were performed to the regions for source and drain electrodes to form a 150-nm-deep box profile with $Si = 5 \times 10^{19}\,cm^{-3}$, followed by 30-min activation annealing at 925 °C in a N_2 gas atmosphere by using an infrared-lamp annealing system. The near-surface region of the implanted areas had a lower Si density due to the nature of the ion implantation process. To expose the highly doped subsurface layer for direct contact with the ohmic metal, a 13-nm-deep recess was performed to the implanted regions by BCl_3 reactive ion etching (RIE) at chamber pressure of 5.0 Pa and plasma power of 100 W prior to evaporation of Ti(20 nm)/Au(230 nm) and liftoff. To further reduce the contact resistance, the Ti/Au metal stack was annealed at 470 °C for 1 min in N_2 by using a rapid thermal annealing system. As shown in Fig. 2(a), the annealed Ti/Au contacts on an implanted Ga_2O_3 film with $Si = 5 \times 10^{19}\,cm^{-3}$ were ohmic with linear *I–V* behavior whereas the non-annealed ones showed weak Schottky behavior. The specific contact resistance of the annealed electrodes as measured by the circular transmission-line method was as low as $8.1 \times 10^{-6}\,\Omega \cdot cm^2$, which is comparable to typical values for conventional Ti/Al-based alloyed contacts on *n*-GaN and/or AlGaN/GaN heterostructures. Cross-sectional transmission electron microscopy (TEM) revealed a defective Ga_2O_3 region and a reacted Ti–Ga_2O_3 region at the annealed Ti/Ga_2O_3 interface [Fig. 2(b)]. We speculate that these interfacial reactions contributed to the improved contact ohmicity. Further details of the Si^+ implantation doping in β-Ga_2O_3 and its application to fabrication of low-resistance ohmic contacts have been reported elsewhere.[16] Next, a 20-nm-thick Al_2O_3 gate dielectric and passivation film was formed on the Ga_2O_3 layer by plasma-assisted ALD at 250 °C using trimethylaluminum and oxygen plasma. The inductively coupled plasma (ICP) power was 300 W, the O_2 gas flow rate was 20 sccm, and the Al_2O_3 deposition rate was 0.9 Å/cycle. The gate metal was formed with Ti(3 nm)/Pt(12 nm)/Au(280 nm) on top of the Al_2O_3 film. Probing pads of the source and drain electrodes were subsequently opened by BCl_3 ICP-RIE. We fabricated and characterized two types of devices with a gate length (L_g) of 2 or 4 μm. The gate width, source-drain implant spacing, and diameter of the inner circular drain electrode were 500, 20, and 200 μm, respectively.

Figure 3(a) shows the DC *I-V* curves of the Ga_2O_3 MOSFET with $L_g = 2$ μm measured at RT. The I_d was effectively modulated by the gate voltage (V_g) with good saturation and sharp pinch-off characteristics. The maximum I_d was 39 mA/mm for $V_g = +4$ V. Device self-heating caused by the poor thermal conductivity of the Ga_2O_3 substrate gave rise to the negative output conductance with increasing drain voltage (V_d). The three-terminal off-state V_{br}, limited by catastrophic dielectric breakdown at the drain side of the gate, was as large as 370 V at $V_g = -20$ V. Figure 3(b) shows the RT transfer characteristics of the MOSFET for $V_d = 25$ V. The I_d on/off ratio was extremely high, exceeding ten orders of magnitude with the measured off-state leakage of a few pA/mm reaching the lower limit of the measurement instrument. These Ga_2O_3 MOSFET characteristics were superior to those of the Ga_2O_3 MESFETs we had reported previously,[1] which we attribute to not only the large decrease in the contact resistance with Si^+-implanted source and drain electrodes but also the low leakage current owing to the Al_2O_3 gate dielectric.



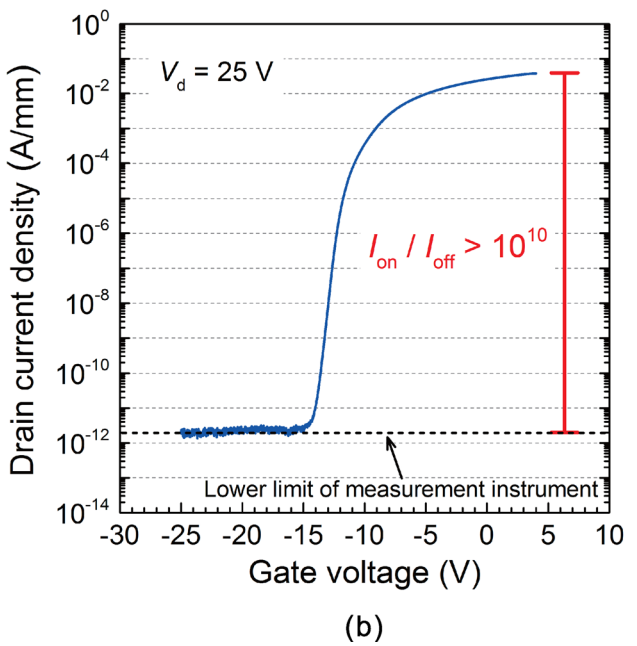
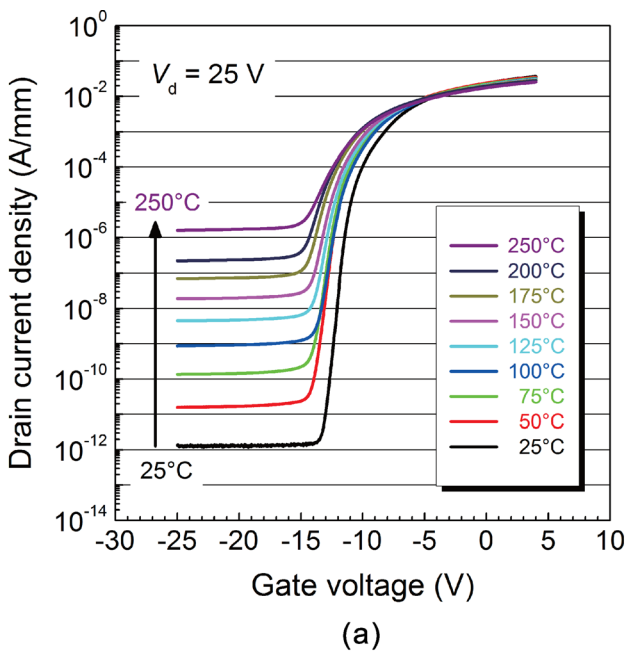


FIG. 3. (a) DC *I-V* curves and (b) transfer characteristics at $V_d = 25$ V of Ga_2O_3 MOSFET ($L_g = 2$ μm) measured at RT.

Next, we investigated the performance of the Ga_2O_3 MOSFET at elevated temperatures. The temperature-dependent measurements were performed in atmosphere by using an on-chip probing setup equipped with a heated sample stage. Figure 4(a) illustrates the temperature-dependent transfer characteristics of the MOSFET with $L_g = 2$ μm at $V_d = 25$ V. The corresponding I_d on/off ratios, defined as the I_d at $V_g = 0$ V divided by the I_d at $V_g = -25$ V, are plotted in Fig. 4(b). These device characteristics evolved smoothly with increasing device operating temperature. No kinks or abrupt changes that might be indicative of breakdown events and/or permanent degradation were observed, suggesting stable device operation in the whole temperature range from 25 to 250 °C, despite a modest reduction in the maximum I_d of approximately 30%. The MOSFET maintained a high I_d on/off ratio of approximately 10^4 even at 250 °C as shown in Fig. 4(b). Furthermore, after high-temperature operation at 250 °C and cooling down to RT, the MOSFET exhibited fully recovered device characteristics. Figure 5 plots drain and gate currents (I_d and I_g) under the pinch-off condition of Ga_2O_3 MOSFETs with $L_g = 4$ μm measured at RT and 250 °C. Different-type source-measure units, which had lower detection limits of about 200 and 2 pA/mm, were used for the measurements of I_d and I_g, respectively. In case of the RT operation, both the off-state I_d and I_g remained below the respective detection limits within the applied V_d range up to the device breakdown. Even at 250 °C, the I_d and I_g still kept small values of less than about 20 and 5 μA/mm, respectively. The off-state V_{br} were 404 and 378 V for RT and 250 °C,



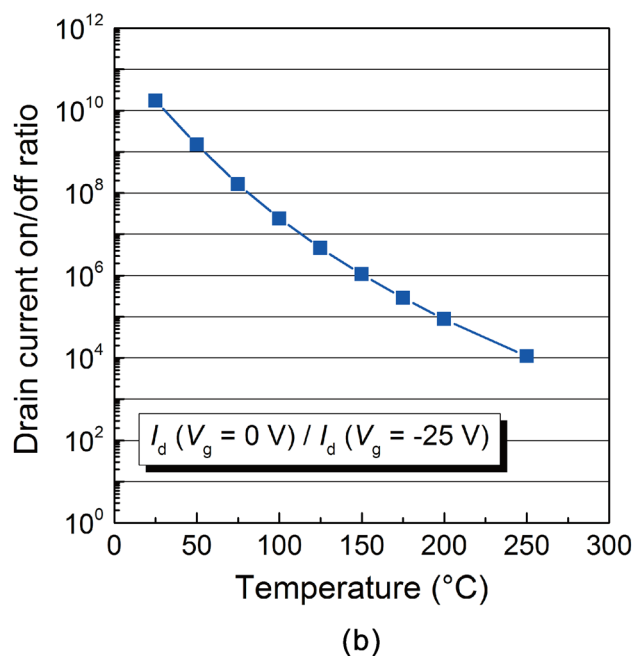


FIG. 4. (a) Transfer characteristics at $V_d = 25$ V and (b) I_d on/off ratios of Ga_2O_3 MOSFET ($L_g = 2$ μm) as a function of operating temperature.

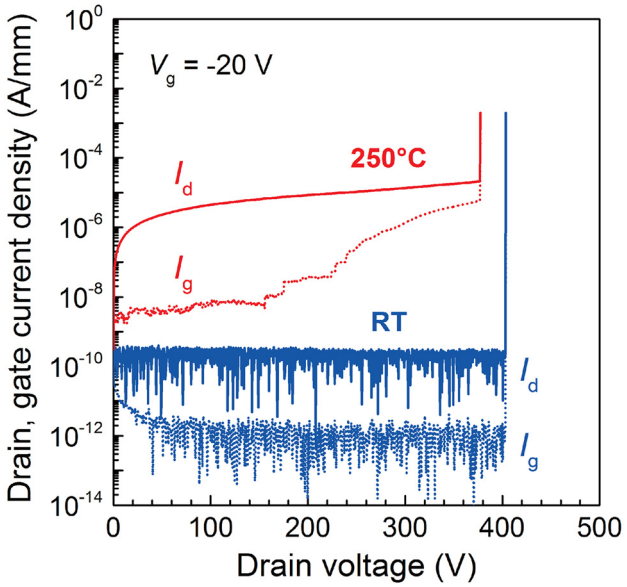


FIG. 5. Off-state breakdown characteristics of Ga_2O_3 MOSFETs ($L_g = 4$ μm) operating at RT and 250 °C; $V_g = -20$ V.

respectively. The device breakdowns occurred at both temperatures were permanent ones caused by destructive degradation of the Al_2O_3 dielectrics and gate electrodes. This is consistent with the I_d and I_g behaviors that increased significantly at the point of V_{br} due to a short-circuiting between the gate and drain electrodes. All these results indicate that the Ga_2O_3 MOSFET can perform at elevated temperatures up to at least 250 °C without noticeable irreversible degradation in electrical characteristics.

In summary, we succeeded in demonstrating depletion-mode Ga_2O_3 MOSFETs on single-crystal β-Ga_2O_3 (010) substrates. Despite a simple device structure, the MOSFETs with $L_g = 2$ μm demonstrated excellent device characteristics represented by a maximum I_d of 39 mA/mm for $V_g = +4$ V, an I_d on/off ratio of over ten orders of magnitude, and a three-terminal V_{br} of 370 V. The devices also showed good performance at 250 °C with no significant permanent degradation. These results demonstrate the great potential of Ga_2O_3 electron devices for power electronics applications in the near future.

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